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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known

Application Number	10/781,383
Filing Date	Feb. 18, 2004
First Named Inventor	Wu, Koucheng
Art Unit	2826
Examiner Name	Minh loan Tran
Attorney Docket Number	KWU003

U. S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

Examiner
Signature Minhloan Tran

Date Considered

5/05

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				Examiner Name	Minhloan Tran
Sheet	1	of	2	Attorney Docket Number	KWU003

NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T ²
MLT	1	M. P. LEPSELTTER and S. M. SZE, "SB-IGFET: An Insulated-Gate Field-Effect Transistor Using Schottky			
		Barrier Contacts for Source and Drain", Proc. IEEE, pp. 1400-1402, Aug. 1968.			
	2	J. R. TUCKER, C. WANG, and P. S. CARNEY, "Silicon Field-Effect Transistor Based on Quantum			
		Tunneling", Appl. Phys. Lett, vol. 65, no. 5, pp. 618-620, Aug. 1994.			
	3	B. WINSTEAD and U. RAVAIOLI, "Simulation of Schottky Barrier MOSFET's with a Coupled Quantum			
		Injection/Monte Carlo Technique", IEEE Trans. Electron Devices, vol. 47, no. 6, pp. 1241-1246,			
		Jun. 2000.			
	4	J. KEDZIERSKI, P. XUAN, E. H. ANDERSON, J. BOKOR, T.-J. KING, and C. HU, "Complementary Silicide			
MLT		Source/Drain Thin-Body MOSFETs for the 20nm Gate Length Regime", IEDM Tech. Digest, pp. 57-60, 2000			

Examiner Signature	Minhloan Tran	Date Considered	5/05
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MLT	5	J. D. PLUMMER and P. B. GRIFFIN, "Material and Process Limits in Silicon VLSI Technology".	
		Proc. IEEE, vol. 89, no. 3, pp. 240-258, 2001.	
	6	D. J. FRANK, R. H. DENNARD, E. NOWAK, P. M. SOLOMON, Y. TAUR, and H.-S. P. WONG, "Device Scaling	
		Limits of Si MOSFETs and Their Application Dependencies", Proc. IEEE, vol. 89, no. 3, pp. 259-288.	
		2001.	
	7	Semiconductor Industry Association, "International Technology Roadmap for Semiconductors	
		2002 Update", 2002.	
	8	Y. ZHANG, J. WANG, L. WANG, and B.-Y. NGUYEN, "Design of 10-nm-Scale Recessed Asymmetric Schottky	
MLT		Barrier MOSFETs", IEEE Electron Device Letters, vol. 23, no. 7, pp. 419-421, 2002.	
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